The 17th ROK-USA Forum on Nanotechnology

Low Power 2D/oxide Memtransistor Device with Highly Reliable Heterosynaptic Plasticity

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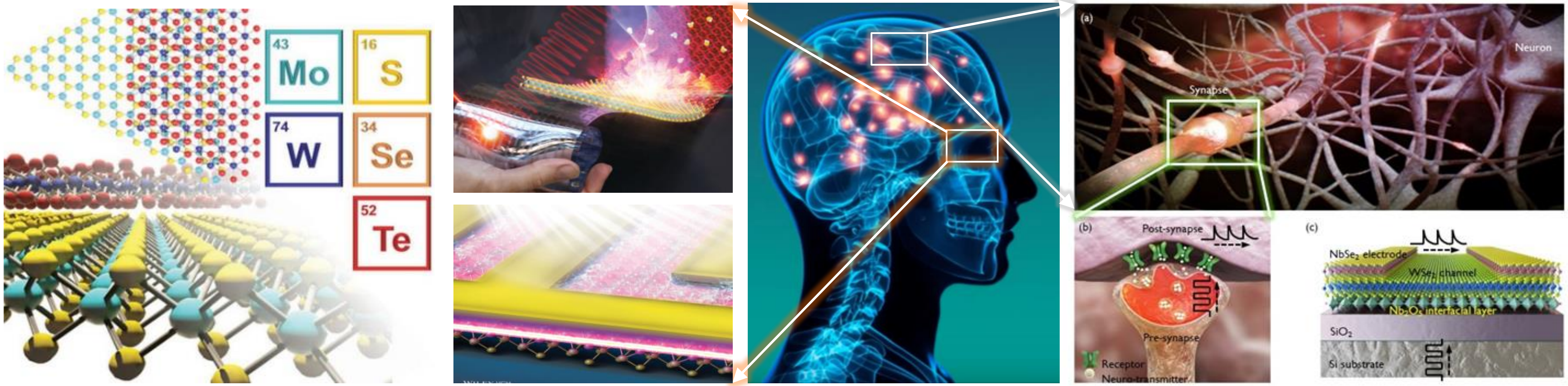
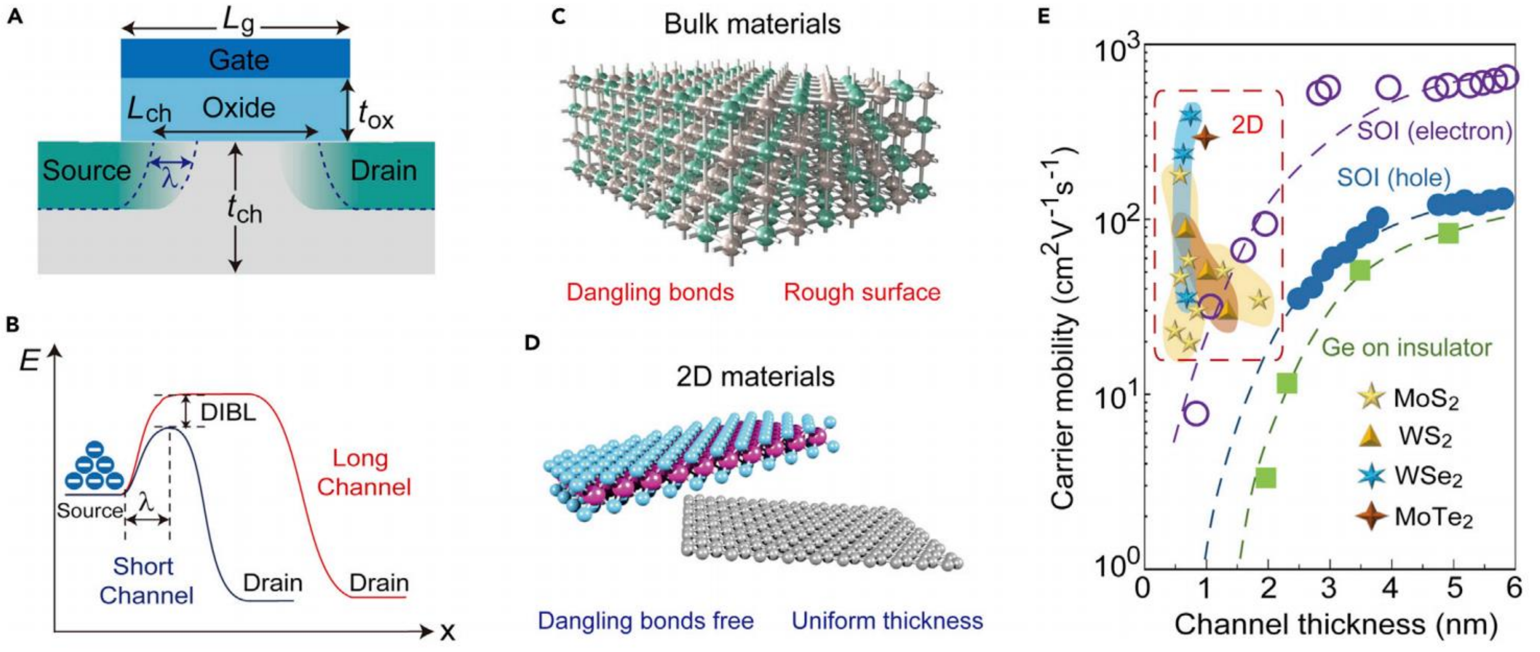
Prof. Byungjin Cho



Scaling immunity of 2D transistors

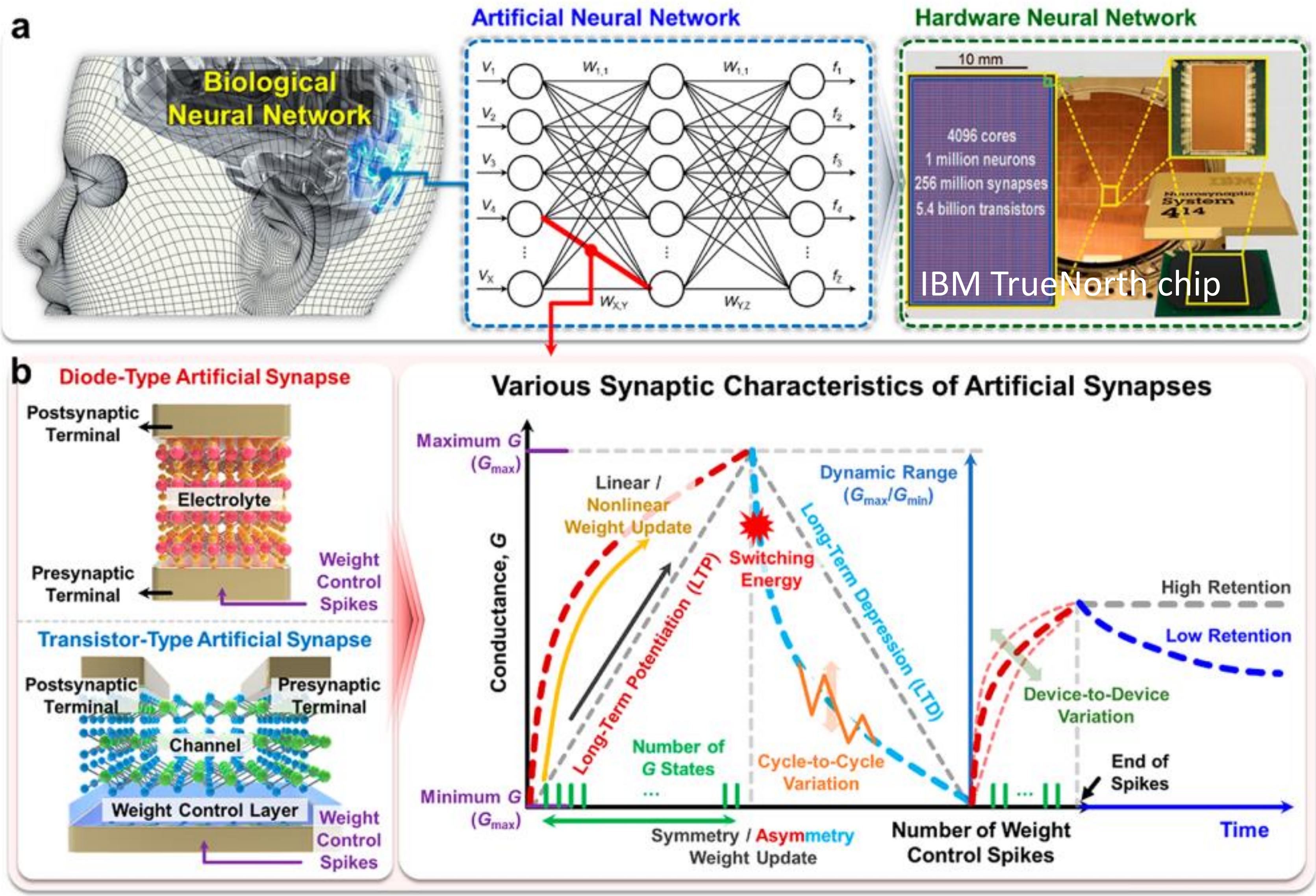


iScience, 25, 105160 (2022)

$$\boxed{\lambda_{2D} = t_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_{ox}} \times t_{ox}}$$

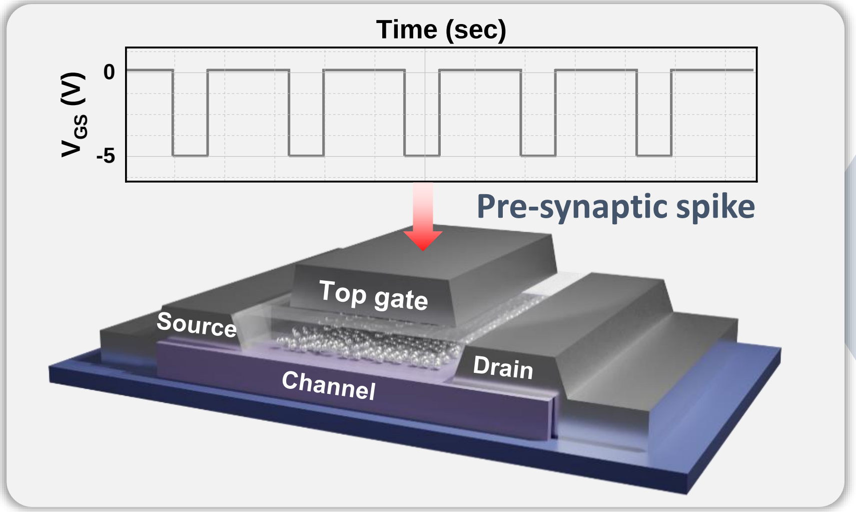
- Scaling length (λ) approaching 1 nm, enabling ultra-short channel transistor
- Dangling bonding free surface and uniform thickness
- Quantum confinement from a limited ‘vertical’ dimension making electrons less prone to scattering
- Rich band structure of the 2D materials

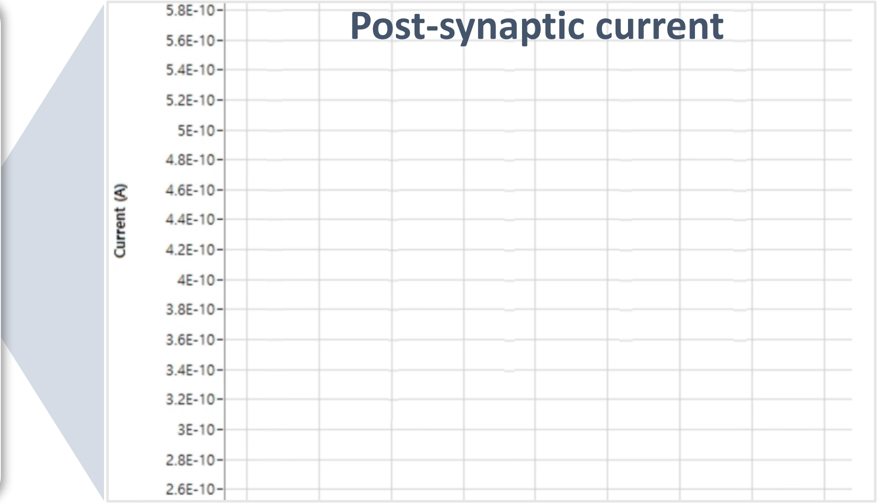
Artificial synapses based on 2D materials



Jin-Hong Park et al., ACS Appl. Electron. Mater. 2, 371 (2020)

Promising candidates for artificial synapse

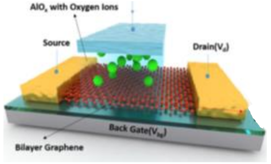




Material candidates

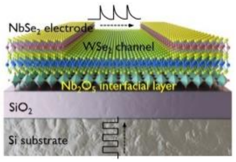
2D materials

Graphene



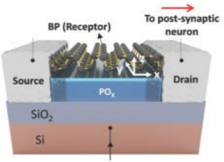
Nano Lett. (2015)

2D TMD



Nanomaterials (2020)

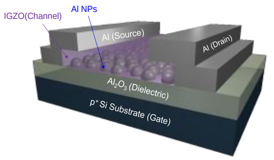
BP



Adv. Mater. (2016)

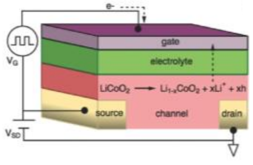
Others

Oxide



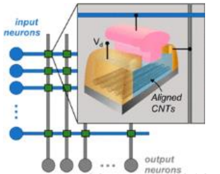
Adv. Electron. Mater. (2020)

Ionic



Adv. Mater. (2017)

CNT

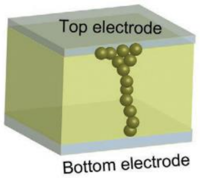


ACS Nano (2018)

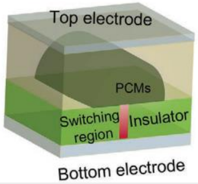
Working mechanisms

Two-terminal

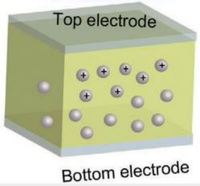
Conductive filament



PCM

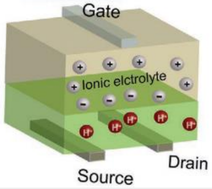


Charge trap (Mem-Tr)

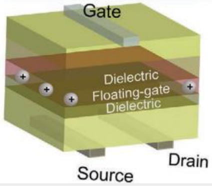


Three-terminal

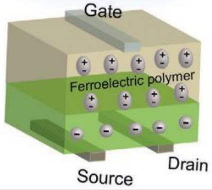
EDL



Charge trap



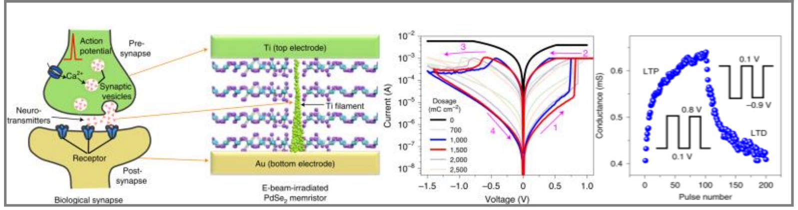
FeFET



Adv. Mater. (2021)

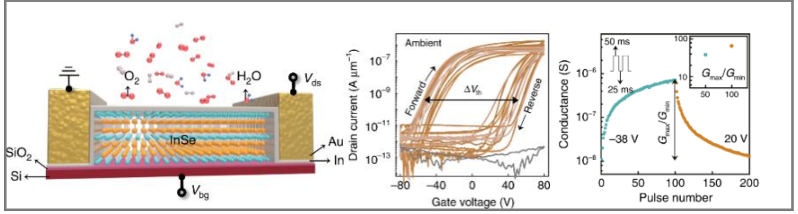
Research motivation: novel 2D memtransistor architecture

Two-terminal memristor

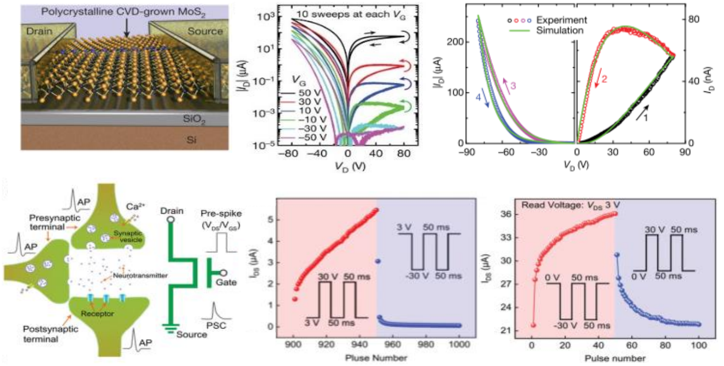


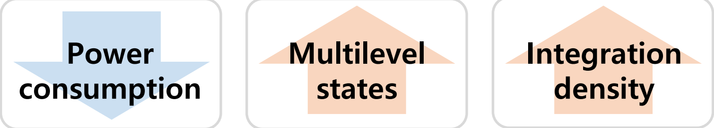
+

Three-terminal transistor



2D Memtransistor



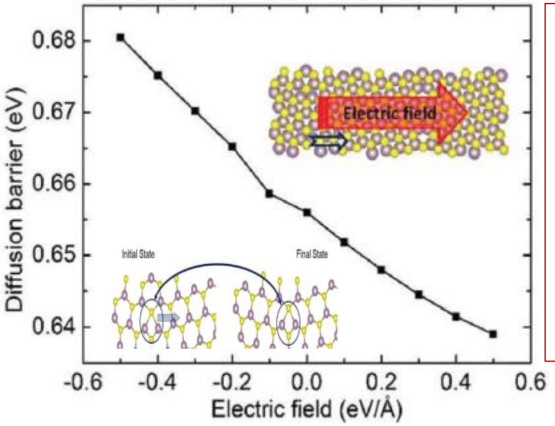


Power consumption

Multilevel states

Integration density

Limitation of Intrinsic sulfur vacancy–based memtransistor

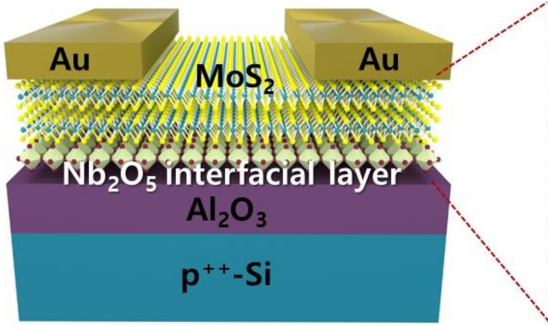


- ✓ difficulty in controlling sulfur vacancy(V_s) concentration and distribution
- ✓ high V_s diffusion energy barrier
- ✓ high operation voltage

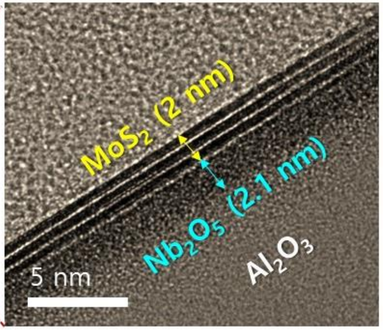
Need to explore another parameter of driving memtransistor switching !!!

Novel 2D/oxide memtransistor architecture

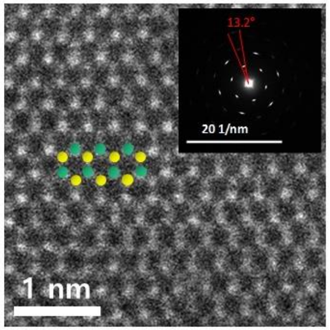
➢ Device structure



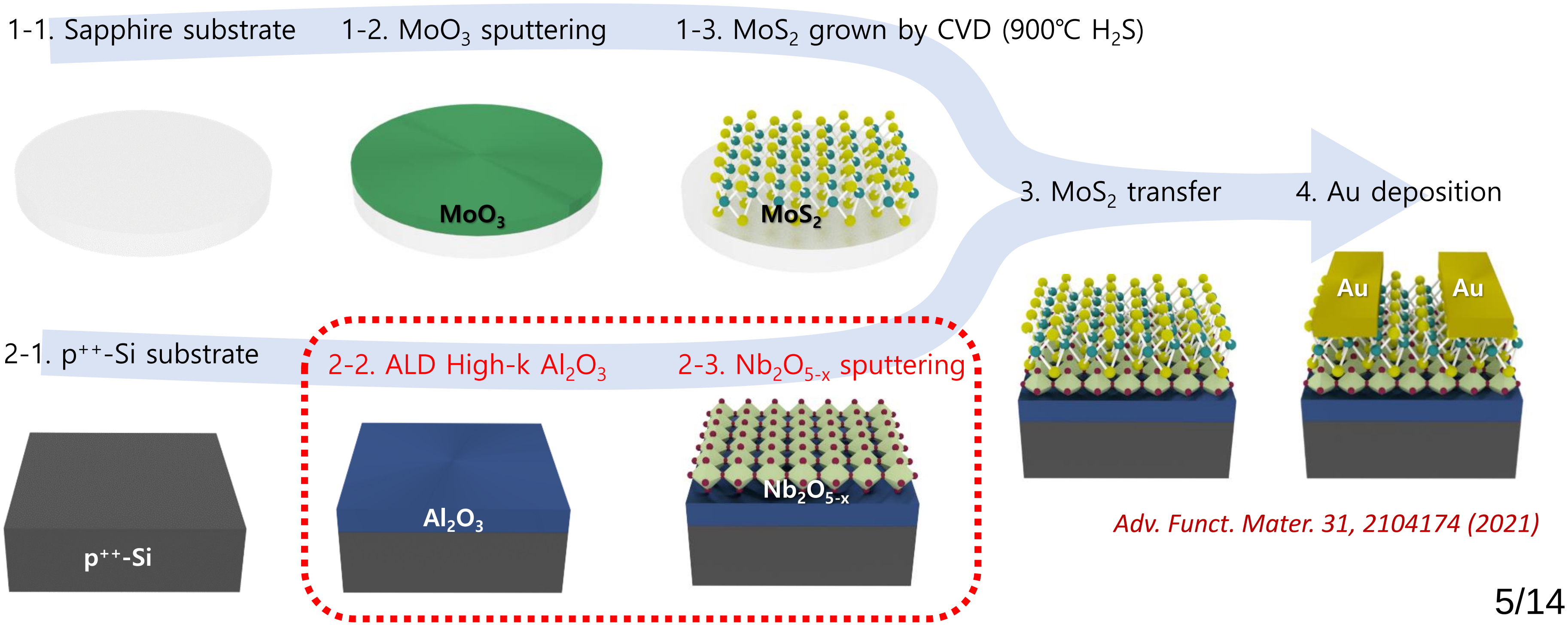
Vertical MoS_2/Nb_2O_{5-x} TEM



Planar MoS_2 TEM



➢ Device fabrication process flow



1-1. Sapphire substrate

1-2. MoO_3 sputtering

1-3. MoS_2 grown by CVD (900℃ H_2S)

2-1. p^{++}-Si substrate

2-2. ALD High-k Al_2O_3

2-3. Nb_2O_{5-x} sputtering

3. MoS_2 transfer

4. Au deposition

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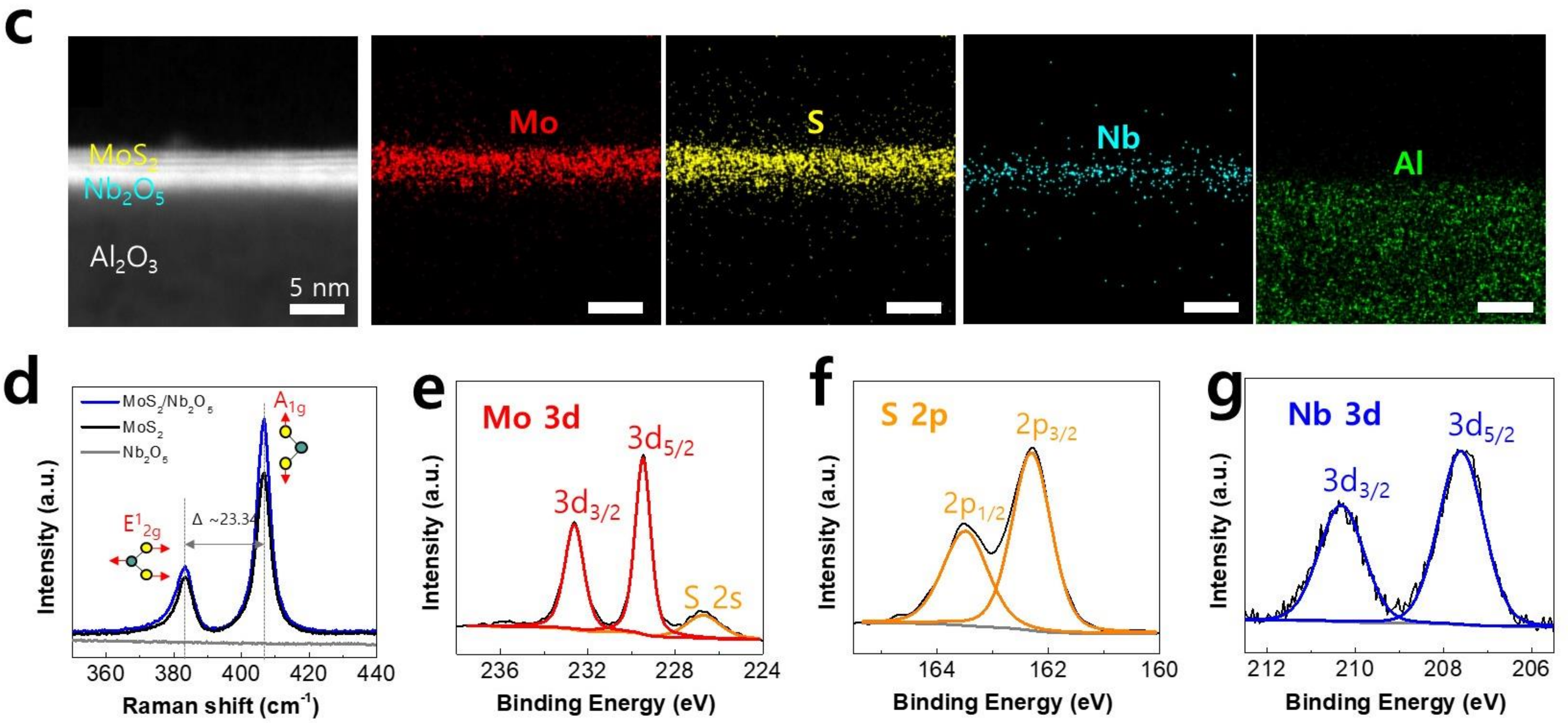
Memtransistor with 2D MoS_2/Nb_2O_{5-x} heterostructure



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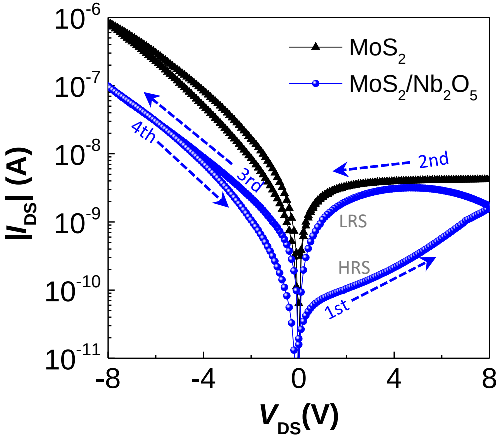
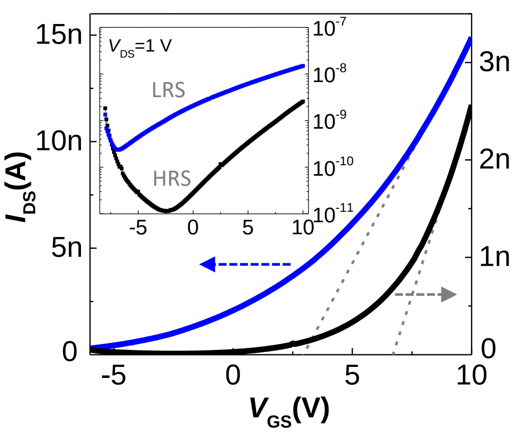
- HRTEM EDS elemental mapping images verify vertically stacked $MoS_2/Nb_2O_{5-x}/Al_2O_3$ films
- Each layer was clearly separated, indicating no formation of the unintentional alloy

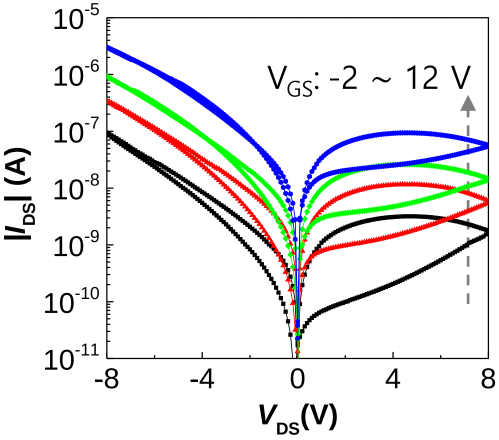
Gate-tunable resistive switching behavior



Resistive switching (V_{DS}-I_{DS})



Transfer curves (V_{GS}-I_{DS})



V_{GS}-dependent V_{DS}-I_{DS}

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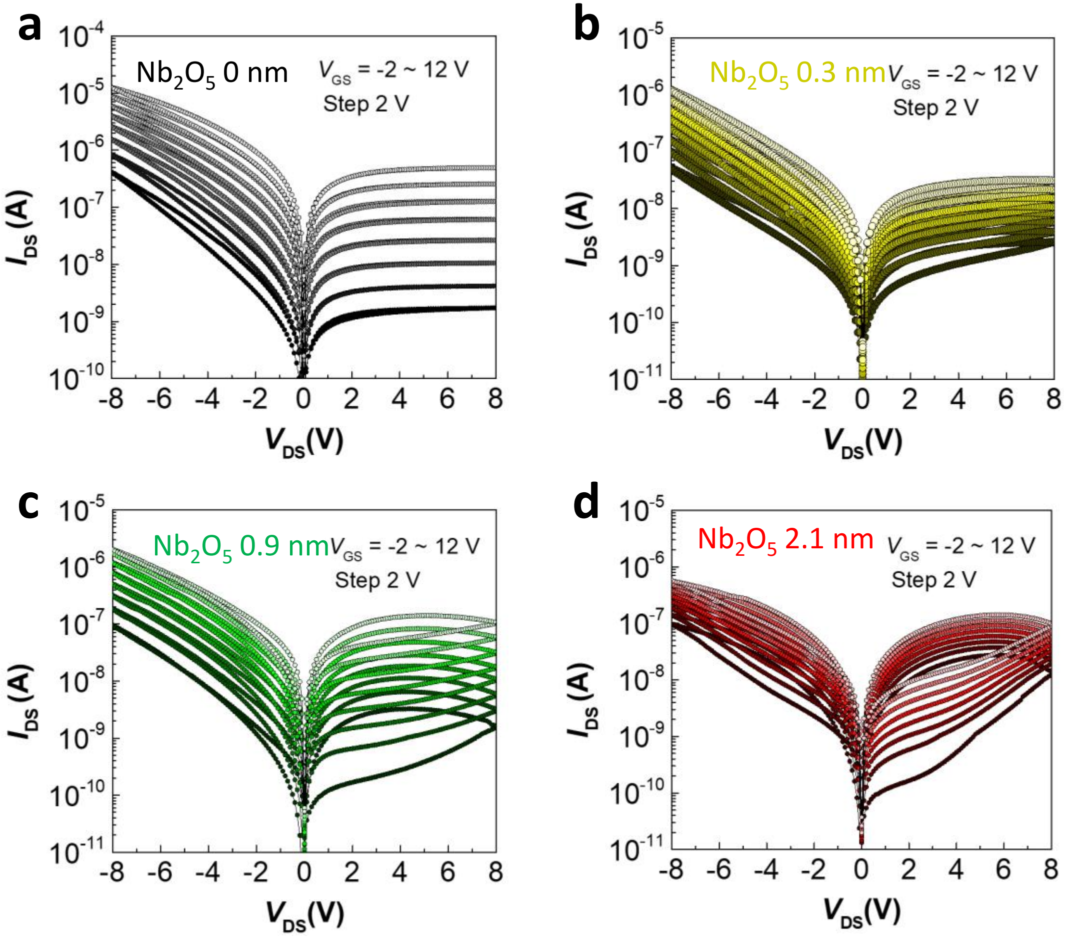
- Introduction of Nb_2O_{5-x} on MoS_2 induced resistive switching
- Bistable resistance states (HRS & LRS) could be made by polarity of V_{DS}
- Gate-tunable resistive switching was well implemented, showing typical memtransistor behavior

Nb_2O_{5-x} thickness dependent memtransistor switching



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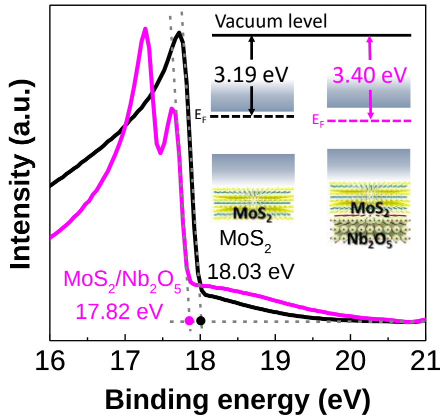
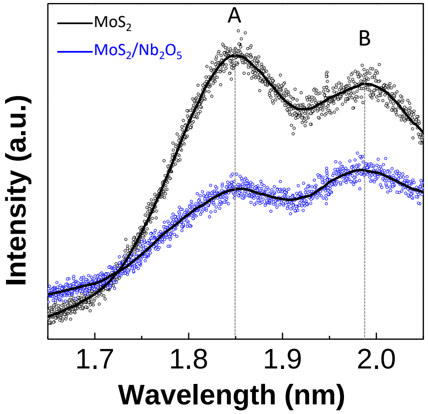
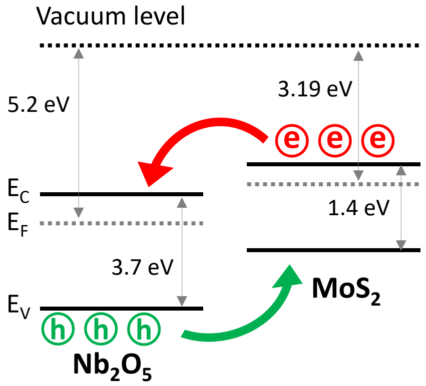
- If considering the tradeoff between the gating efficiency and resistive switching ratio, the memtransistor switching was optimized in the thickness range of approximately 2.1 nm

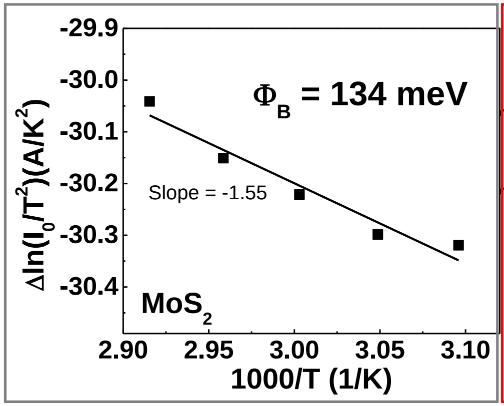
Schottky barrier modulation coming from oxide layer



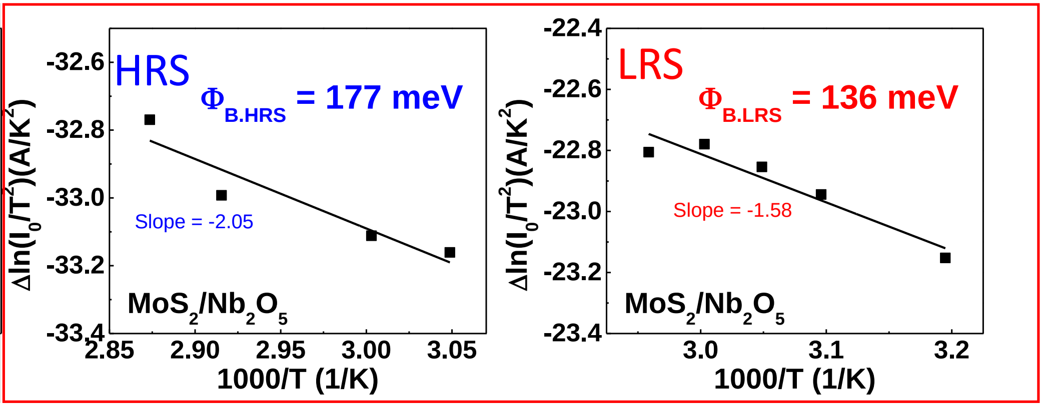




2D transistor



2D memtransistor



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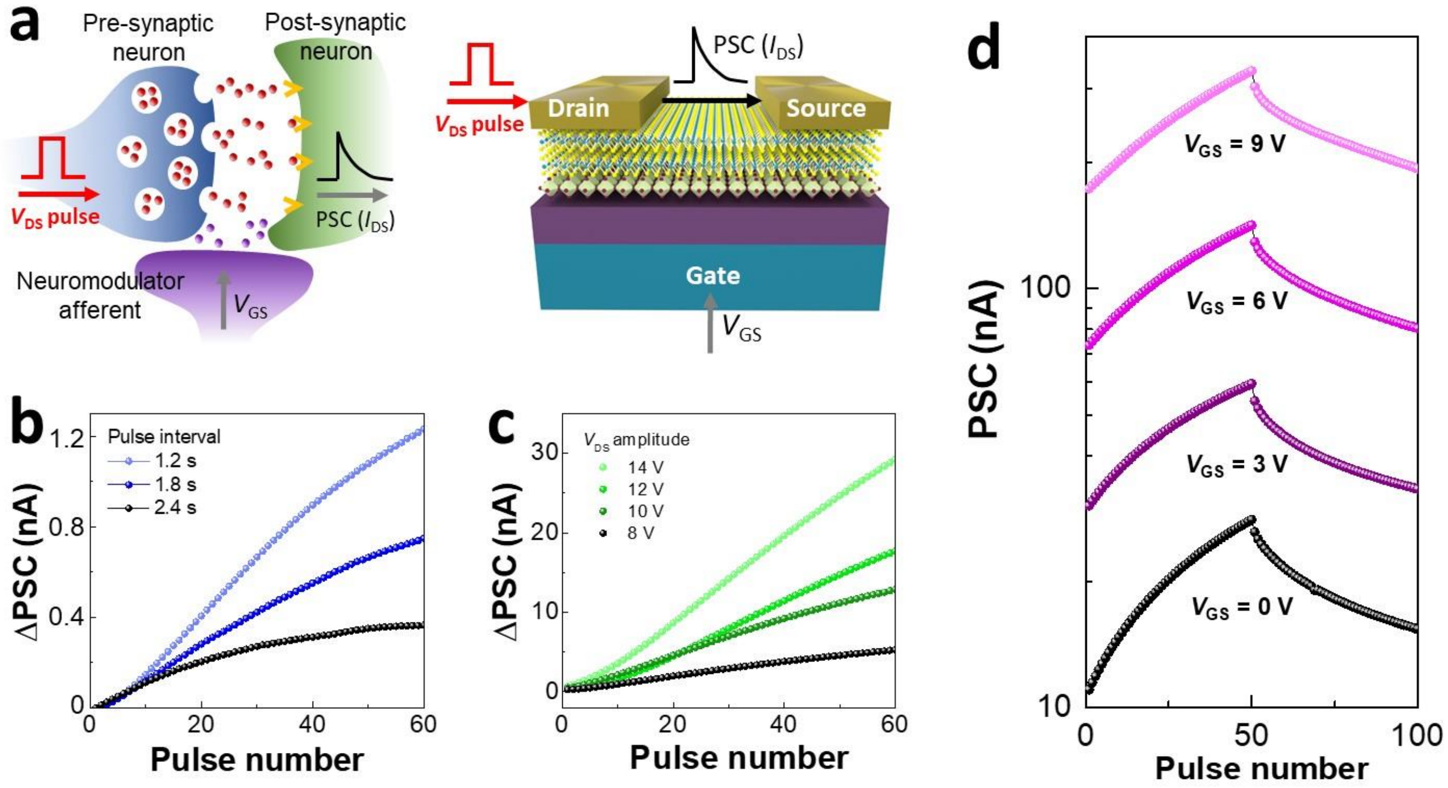
- UPS & PL characterization validate charge transfer between MoS_2 and Nb_2O_{5-x}
- The drain current throughout the MoS_2/ Nb_2O_{5-x} film can be more effectively tuned *via* the modulation of the Schottky barrier height

Drain-terminal tuning of MoS_2/Nb_2O_{5-x} memtransistor



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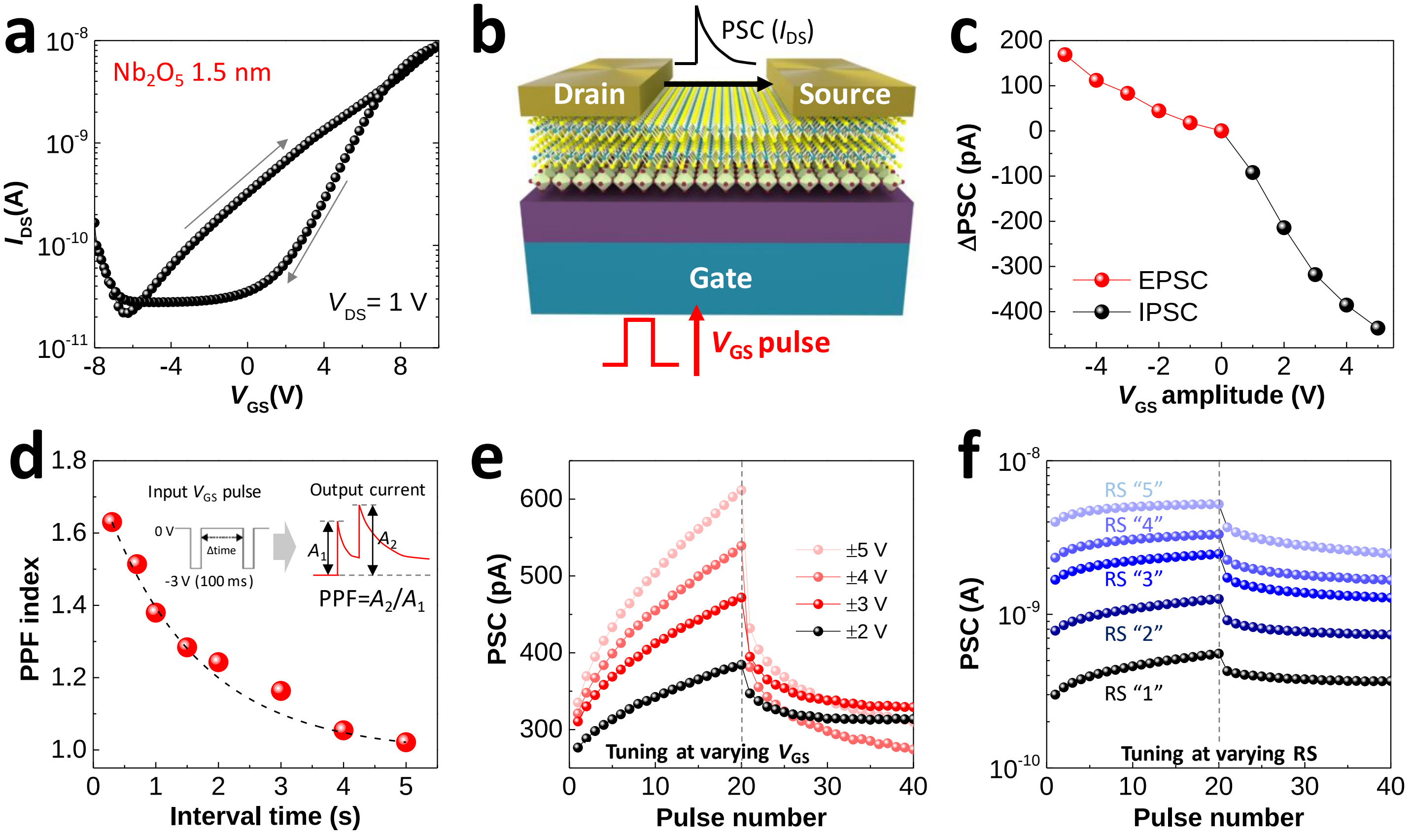
- The activity of a neuromodulator affects the synaptic connection, which is key for heterosynaptic plasticity preventing the instability of the synaptic weight change
- MoS_2/Nb_2O_{5-x} memtransistor with a wide conductance tunability successfully emulated an artificial neuromodulator

Gate-terminal tuning of MoS_2/Nb_2O_{5-x} memtransistor



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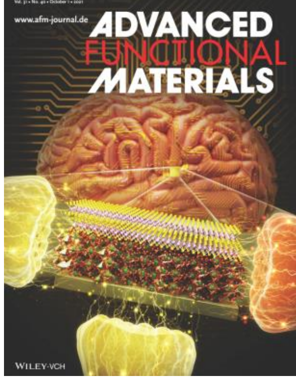
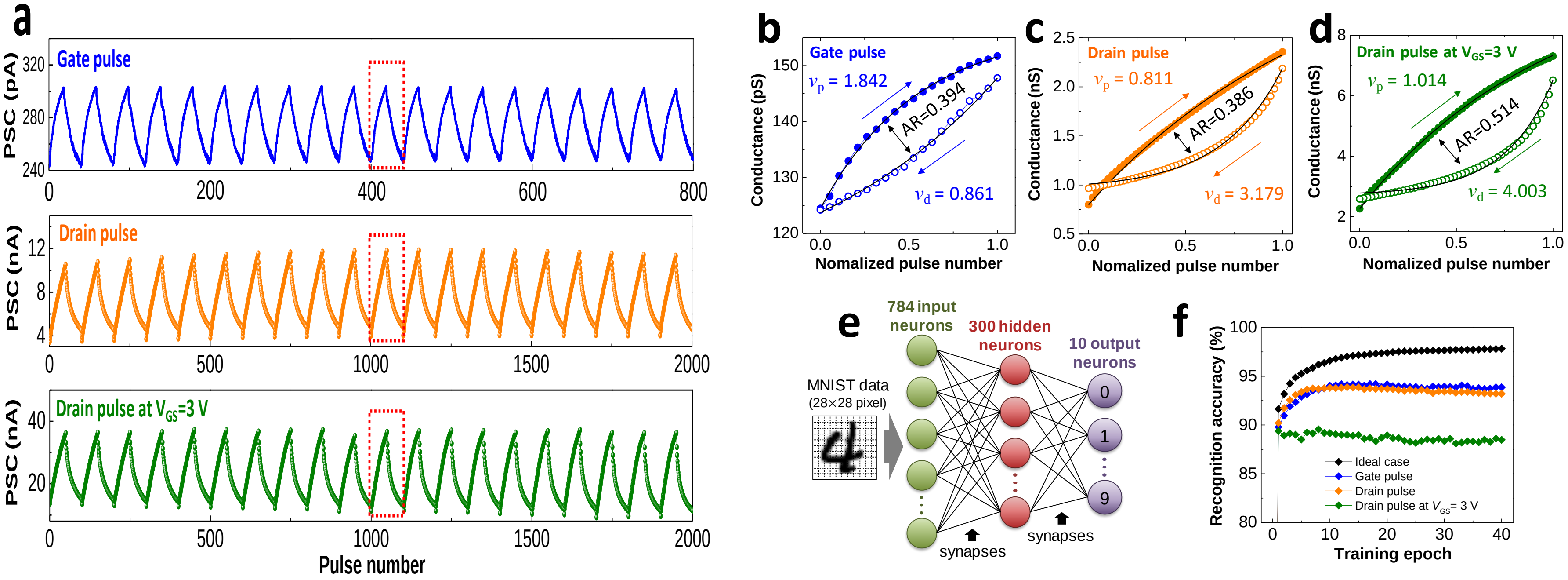
- The Nb_2O_{5-x} with a large amount of oxygen vacancies functions as a charge trapping layer between the MoS_2 channel and the Al_2O_3 high-k dielectric
- Essential synaptic parameters of EPSC, IPSC, PPF, LTP, and LTD were also achieved under variable gate pulse condition

MNIST pattern recognition simulation





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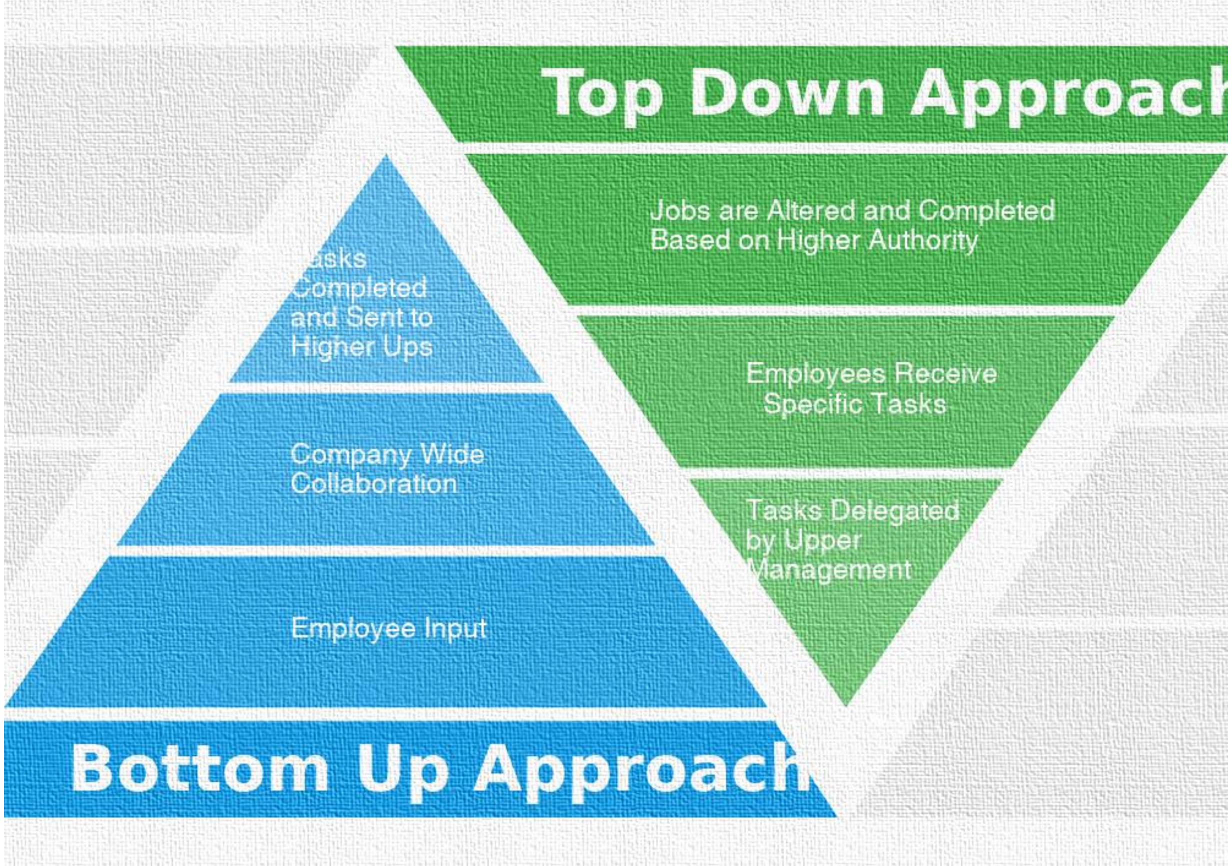
- Best pattern recognition accuracy of neuromorphic system with our 2D MoS_2/Nb_2O_{5-x} would be evaluated to be ~ 94.2 %
- Memtransistor devices show an extremely low power consumption of ~6 pJ in single spike

Conclusion

1. Novel memtransistor architecture was designed using a 2D/oxide simple structure
2. Heterosynaptic plasticity would be useful for the implementation future complex neuromorphic circuit
3. The mechanism of the memtransistor switching is strongly related to the Schoottky barrier height modulation induced by Nb_2O_5 layer
4. Ultra-scalability and unique memetranssitor switching of the 2D materials accelerate the feasibility of massively-connected neuromorphic circuitry in near future.

RoK-USA research cooperation strategy



- We need to initiate the sustainable graduate-student exchange program funded by both USA and Korea government
- Two-track strategy including both bottom-up small and top-down massive project will be able to meet various kinds of the cooperation-type between USA and Korea researchers if possible.

Acknowledgements

➢ Funding sources

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Post−doctor

Graduate students

Undergraduate students

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KIMS

INHA UNIVERSITY

PUSAN NATIONAL UNIVERSITY

KOREA MARITIME AND OCEAN UNIVERSITY

Gwangju Institute of Science and Technology

KOREA BASIC SCIENCE INSTITUTE

EWHA W.U.

Thank you
for your kind attention